UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/504,003	02/14/2000	Opher Kahn	42390.P8517	7395

7590 02/26/2003

Jeffrey S Draeger
Blakely Sokoloff Taylor & Zafman
12400 Wilshire Boulevard
7th FLoor
Los Angeles, CA 90025

EXAMINER
CHANG, ERIC

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 02/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/504,003	KAHN ET AL.	
	Examiner	Art Unit	
	Eric Chang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

1. Claims 1-25 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-5, 7-9, 18-21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,128,747 to Thoulon, in view of U.S. Patent 6,230,274 to Stephens et al.

5. As to claim 1, Thoulon discloses an apparatus comprising:

[a] a processor [col. 3, line 33];

[b] an operating system to control a plurality of power management states, comprising a low latency low power state [col. 1, lines 33-35];

[c] a memory subsystem that exits a memory low power state [col. 2, lines 37-41]; and

[d] control logic to detect exiting of said low latency low power state and to remove said memory subsystem from said memory low power state prior to allowing execution of processor to resume [col. 5, line 37-47].

Thoulon teaches all of the limitations of the claim, by allowing for resumption of memory operations from a low latency sleep state by means of control logic that does not require BIOS intervention, but does not teach the specific initialization commands required by the memory subsystem to exit the low power state.

Stephens teaches a series of initialization commands to bring a memory system out of a low power state [col. 21, lines 16-20]. Stephens also teaches that these commands are performed by the initialization of the memory modules [col. 16, lines 17-55]; logic to perform these tasks may be controlled by the memory controller, and therefore independent of the BIOS.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the initialization commands as taught by Stephens. One of ordinary skill in the art would have been motivated to do so to properly initialize the memory when it exits from the low power state.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of exiting a memory from a low power state. Moreover, the initialization means taught by Stephens would improve the utility of Thoulon because it allowed the teachings of Thoulon to be applied to a memory that requires a significant amount of initialization, wherein the initialization is specified to include the steps taught by Stephens.

6. As to claim 2, Thoulon discloses the resumption from low power mode is performed by control logic in the memory controller and does not require executing BIOS or other firmware routines [col. 4, lines 2-14].

7. As to claim 3, Thoulon discloses the low power state is one as defined by the ACPI standard where STPCLK is asserted, as in the S1 state [col. 1, lines 33-47]. Furthermore, Thoulon teaches that during the sleep state, other processes may occur independently of the processor, meaning that although the system is in a low power state, context is maintained, as in the S1 state, substantially as claimed [col. 5, lines 1-6].

8. As to claims 4-5, 18 and 24, Thoulon discloses the control logic detects exit from the low power state [col. 4, lines 39-50 and 59-67], and deasserts the stop clock signal after the memory capabilities have been resumed [col. 4, lines 51-58]. Thoulon also teaches that this process occurs transparently to the execution resources of the processor [col. 4, lines 9-14]. In addition, Stephens specifies the initialization commands needed to exit the memory from the low power state [col. 21, lines 16-20]. Furthermore, it would be obvious to one of ordinary skill in the art that the means by which Stephens teaches detecting a suspend terminating event [col. 21, line 11], or any like method, may be used instead of the means by which Thoulon accomplishes the same, because they are both directed towards determining when a memory should be brought out of a low power mode.

9. As to claims 7 and 19, Stephens discloses the initialization commands comprise:

[a] initializing memory interface control logic [col. 21, line 24];

[b] starting a clock [col. 21, lines 23];

[c] performing a current calibration sequence [col. 21, lines 27-28]; and

[d] performing memory core initialization operations [col. 21, lines 25-26].

Furthermore, Stephens teaches starting the clock comprises waiting for the clock circuit to lock [col. 12, lines 5-6], and that performing a current calibration sequence comprises setting a control current register [col. 16, lines 28-31], substantially as claimed.

10. As to claims 8 and 20, Stephens discloses setting the current control register to a midpoint value [col. 16, lines 33-40].

11. As to claims 9 and 21, Stephens discloses the core initialization comprises performing a series of pre-charge and refresh operations [col. 16, lines 41-50].

Claim Rejections - 35 USC § 103

12. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

13. Claims 6, 10-17, 22-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,128,747 to Thoulon, in view of U.S. Patent 6,230,274 to Stephens et al., and in further view of U.S. Patent 6,272,642 to Pole, II et al.

14. As to claim 6, Thoulon teaches that the sleep control means are incorporated in the memory controller, which may comprise a memory interface and ICH, substantially as claimed [col. 6, lines1-3]. Stephens also teaches a low power state exit message [col. 8, line 67 and col.

9, line 1] and signaling that the memory interface has completed its initialization commands [col. 4, lines 30-33]. Thoulon and Stephens teach all of the limitations of the claim, but do not specifically teach the messaging logic between the ICH and the memory interface.

Pole teaches that messages, such as those pertaining to placing the system into sleep modes, may be used to communicate between memory and I/O hubs [col. 4, lines 10-21]. Thus, Pole teaches logic for transmitting messages indicating the claimed contents, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the messaging system as taught by Pole. One of ordinary skill in the art would have been motivated to do so that the memory interface and the ICH are able to communicate with each other.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of communicating sleep commands between a memory interface and an ICH. Moreover, the messaging means taught by Pole would improve the flexibility of Thoulon and Stephens because it allowed direct messaging between the memory interface and the ICH instead of relying on polling a completion register or on direct signals between the two components.

15. As to claims 10-13, Stephens discloses:

[a] low power state exit detection logic [col. 21, line 11];

[b] memory resume logic [col. 21, lines 16-20];

[c] signaling that the memory interface has completed its initialization commands [col. 4, lines 30-33]; and

[d] low power state exit message [col. 8, line 67 and col. 9, line 1].

In addition, Thoulon discloses deasserting the stop clock signal after the memory capabilities have been resumed from a low latency sleep state, substantially as claimed [col. 4, lines 51-58].

Thoulon and Stephens teach all of the limitations of the claim, but do not specifically teach the messaging logic between the ICH and the memory interface.

Pole teaches that messages, such as those pertaining to placing the system into sleep modes, may be used to communicate between memory and I/O hubs [col. 4, lines 10-21]. Thus, Pole teaches logic for transmitting messages indicating the claimed contents, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the messaging system as taught by Pole. One of ordinary skill in the art would have been motivated to do so that the memory interface and the ICH are able to communicate with each other.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of communicating sleep commands between a memory interface and an ICH. Moreover, the messaging means taught by Pole would improve the flexibility of Thoulon and Stephens because it allowed direct messaging between the memory interface and the ICH instead of relying on polling a completion register or on direct signals between the two components.

16. As to claim 14, Thoulon discloses the low power state is one as defined by the ACPI standard where STPCLK is asserted, as in the S1 state [col. 1, lines 33-47]. Furthermore, Thoulon teaches that during the sleep state, other processes may occur independently of the processor, meaning that although the system is in a low power state, context is maintained, as in the S1 state, substantially as claimed [col. 5, lines 1-6].

17. As to claim 15, Stephens discloses the initialization commands comprise:

[a] initializing memory interface control logic [col. 21, line 24];

[b] starting a clock [col. 21, lines 23];

[c] performing a current calibration sequence [col. 21, lines 27-28]; and

[d] performing memory core initialization operations [col. 21, lines 25-26].

Furthermore, Stephens teaches starting the clock comprises waiting for the clock circuit to lock [col. 12, lines 5-6], and that performing a current calibration sequence comprises setting a control current register [col. 16, lines 28-31], substantially as claimed.

18. As to claim 16, Stephens discloses setting the current control register to a midpoint value [col. 16, lines 33-40].

19. As to claim 17, Stephens discloses the core initialization comprises performing a series of pre-charge and refresh operations [col. 16, lines 41-50].

20. As to claim 22, Pole discloses:

[a] reading a bit set by BIOS upon entry into a low latency low power state [col. 7, lines 51-55]; and

[b] sending a resume message from an ICH to memory interface logic [col. 8, lines 25-32].

Pole teaches that messages may be used to communicate between memory and I/O hubs in lieu of signals [col. 4, lines 10-21]. Thus, Pole teaches logic for transmitting messages indicating the detection of an exit from the low power state, substantially as claimed.

21. As to claim 23, Stephens discloses signaling that the memory interface has completed its initialization commands [col. 4, lines 30-33]. In addition, Thoulon discloses deasserting a stop clock signal [col. 4, lines 51-58].

22. As to claim 25, Pole discloses:

[a] detecting a low power state entry [col. 1, lines 36-38]; and

[b] setting a bit to indicate the low latency low power state is selected [col. 6, lines 61-67].

Pole teaches writing a pre-defined value to a control register to indicate the new power state of the processor; this can comprise setting a bit to indicate said selected power state.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ec
February 20, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100